Master's Thesis

An Optimal Gate Design for the Synthesis of Ternary Logic Circuits

Sunmean Kim

Department of Electrical Engineering

Graduate School of UNIST

2018

An Optimal Gate Design for the Synthesis of Ternary Logic Circuits

Sunmean Kim

Department of Electrical Engineering

Graduate School of UNIST

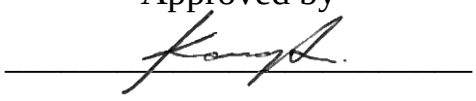
An Optimal Gate Design for the Synthesis of Ternary Logic Circuits

A thesis
submitted to the Graduate School of UNIST
in partial fulfillment of the
requirements for the degree of
Master of Science

Sunmean Kim

12/14/2017

Approved by



Advisor
Seokhyeong Kang

An Optimal Gate Design for the Synthesis of Ternary Logic Circuits

Sunmean Kim

This certifies that the thesis of Sunmean Kim is approved.

12/14/2017 of submission

signature

Advisor: Seokhyeong Kang

signature

Jaehyouk Choi: Thesis Committee Member #1

signature

Seong-Jin Kim: Thesis Committee Member #2

Abstract

Over the last few decades, CMOS-based digital circuits have been steadily developed. However, because of the power density limits, device scaling may soon come to an end, and new approaches for circuit designs are required. Multi-valued logic (MVL) is one of the new approaches, which increases the radix for computation to lower the complexity of the circuit. For the MVL implementation, ternary logic circuit designs have been proposed previously, though they could not show advantages over binary logic, because of unoptimized synthesis techniques.

In this thesis, we propose a methodology to design ternary gates by modeling pull-up and pull-down operations of the gates. Our proposed methodology makes it possible to synthesize ternary gates with a minimum number of transistors. From HSPICE simulation results, our ternary designs show significant power-delay product reductions; 49 % in the ternary full adder and 62 % in the ternary multiplier compared to the existing methodology. We have also compared the number of transistors in CMOS-based binary logic circuits and ternary device-based logic circuits

We propose a methodology for using ternary values effectively in sequential logic. Proposed ternary D flip-flop is designed to normally operate in four-edges of a ternary clock signal. A quad-edge-triggered ternary D flip-flop (QETDFF) is designed with static gates using CNTFET. From HSPICE simulation results, we have confirmed that power-delay-product (PDP) of QETDFF is reduced by 82.31 % compared to state of the art ternary D flip-flop. We synthesize a ternary serial adder using QETDFF. PDP of the proposed ternary serial adder is reduced by 98.23 % compared to state of the art design.

Contents

List of Figures

List of Tables

Acknowledgments

I would like to thank all of the people who helped make this dissertation possible.

First and foremost, I am thankful to my advisor, Professor Seokhyeong Kang, whose guidance, encouragement and support enabled me to complete my Master course and this thesis. His enthusiasm and passion always stimulate me, and his attitude on research will remain as a priceless lesson in my life.

I certainly feel lucky to have worked with many bright colleagues in Professor Kang's System-on-Chip Design Lab. I would like to thank current members Seungwon Kim, Yesung Kang, Jaewoo Kim, Sanggi Do, Mingyu Woo, Taeho Lim, and Segi Lee and former members M.S. Jaemin Lee. We had wonderful projects, and we spent great times together. I wish them the best in their future.

I would also like to thank my thesis committee members, Prof. Jaehyouk Choi and Prof. Seong-Jin Kim for taking time out of their busy schedules to review and evaluate my research work.

Last, but not least, I would like to thank my parents, Hong Goo Kim and Hae Sook Park, and the rest of my family for their endless love and encouragement. Thank you to Daeun Choi, for all her love and support. This thesis is dedicated to them.

The material in this thesis is based on the following publications.

• Chapter III, IV are based on:

– **Sunmean Kim**, Taeho Lim, and Seokhyeong Kang, "An Optimal Gate Design for the Synthesis of Ternary Logic Circuits", *Proc. IEEE/ACM Asia and South Pacific Design Automation Conference*, 2018, accepted.

• Chapter V are based on:

– **Sunmean Kim**, Segi Lee, and Seokhyeong Kang, "Design of Quad-Edge-Triggered Sequential Circuits with a Ternary Clock Signal", *Proc. IEEE International Symposium on Multiple-Valued Logic*, 2018, submitted.

My coauthors (Taeho Lim and Segi Lee) have all kindly approved the inclusion of the aforementioned publications in my thesis.

VITA

1992 Born, Gwangju, South Korea

2016 B.S., Electrical and Computer Engineering,

Ulsan National Institute of Science and Technology, Ulsan, South Korea

• **Sunmean Kim**, Segi Lee, and Seokhyeong Kang, "Design of Quad-Edge-Triggered Sequential Circuits with a Ternary Clock Signal", *Proc. IEEE International Symposium on Multiple-Valued Logic*, 2018, submitted.

• **Sunmean Kim**, Taeho Lim, and Seokhyeong Kang, "An Optimal Gate Design for the Synthesis of Ternary Logic Circuits", *Proc. IEEE/ACM Asia and South Pacific Design Automation Conference*, 2018, accepted.

• Yesung Kang, Jaewoo Kim, **Sunmean Kim**, Sunhae Shin, E-San Jang, Jae Won Jeong, Kyung Rok Kim, and Seokhyeong Kang, "A Novel Ternary Multiplier Based on Ternary CMOS Compact Model", *Proc. IEEE International Symposium on Multiple-Valued Logic*, 2017.

• Jaemin Lee, **Sunmean Kim**, Youngmin Kim, and Seokhyeong Kang, "A novel design methodology for error-resilient circuits in near-threshold computing", *Proc. IEEE International Conference on Consumer Electronics-Asia*, 2017.

Chapter I

Introduction

Up to now, CMOS-based digital system has been improved with the continuous device scaling. However, power density limits prevent further device scaling and new approaches for circuit designs are required [1]. Multi-valued logic (MVL) is one of the new approaches to fundamentally solve the circuit complexity of binary system. MVL allows logic gates to process more values, and is able to implement the same circuit with fewer elements and interconnect wires. Therefore, the MVL can achieve smaller area and less power consumption compared to the binary logic.

Ternary (three-valued) logic is the first step of the MVL, several ternary devices have been studied to realize ternary digital circuits. To implement a ternary gate, multi-threshold voltage (Vth) logic has been exploited with CMOS [2] or carbon nanotube FET (CNTFET) [3]. In quantum-dot gate FET (QDGFET) [4], the multi-Vth has been physically embedded in a single device gate stack to reduce the circuit complexity. Ternary CMOS (T-CMOS) has been proposed which is a CMOS-compatible ternary device technology [5]. Meanwhile, there have been relative few researches on design methodology for the ternary devices, especially, ternary gate design and logic synthesis. Since the conventional synthesis methodology cannot consider the special characteristics of the ternary devices, research is necessary on the ternary logic synthesis.

Logic synthesis is a process of circuit design that satisfies a given truth table. The truth table of binary logic can be converted into a sum-of-products (SOP) expression and then it is optimized to implement the circuit design. However, the truth table of ternary logic consists of three values and cannot be converted into a SOP expression. Therefore, a logic synthesis methodology which converts the ternary values to binary values has been proposed [6]. Based on this approach, a gate design methodology using diode connected transistors instead of resistors has been proposed. Various gate designs have been proposed to reduce the number of transistors subsequently. However, the proposed designs have been optimized for specific circuits such as ternary adders and ternary multipliers, making it difficult to optimally implement ternary logic circuits at the system level. Recently, a ternary logic synthesis methodology based on multiplexers using a transmission gate has been proposed to synthesize a general logic design [7]. However, transmission gates have worse power, speed, and noise margin than static gates. Also, design of ternary logic which improve temporal data density has not been studied sufficiently.

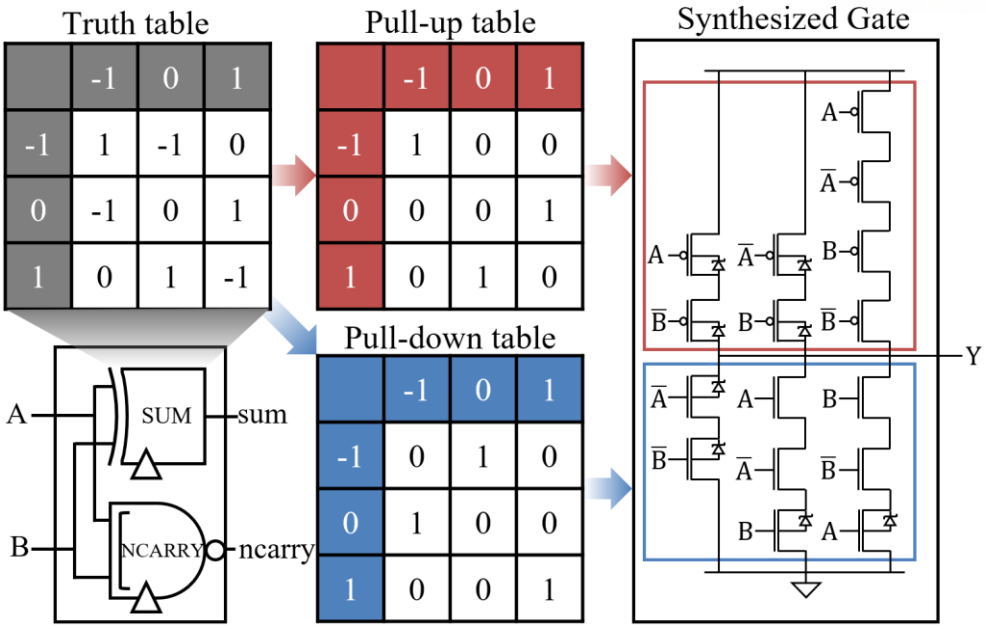


Fig. 1. An optimal static gate design methodology for the synthesis of ternary logic using emerging devices. This example shows the SUM gate of the half adder for balanced ternary logic synthesized in T-CMOS.

In this thesis, we propose an optimal static gate design methodology for the synthesis of ternary logic using emerging devices. As shown in Fig. 1, we build pull-up/pull-down tables from the truth table of ternary logic, and generate an optimal gate circuits based on the switching tables. Our proposed methodology is applicable to all emerging devices supporting ternary logic such as CNTFET, QDGFET, and T-CMOS. Ternary logic circuits generated from our design methodology show significant reduction on the number of transistors compared to binary logic circuits. In addition, while previous studies were limited to standard ternary logic design, this study can be applied to balanced ternary logic [14].

We propose a design of static ternary sequential circuits with ternary clock inverter using CNTFET. As shown in Fig. 2., we use a ternary clock signal instead of a binary clock signal. A ternary clock signal contains four clock edges, 0 to 1, 1 to 2, 2 to1, and 1 to 0. Thus, ternary sequential circuits can be triggered four times in one period of the clock signal. Ternary clock inverter allows ternary sequential circuit to operate at quad-edges of the ternary clock signal. We expect that the ternary clock signal can be generated from a sinusoidal signal with the same period of a binary clock signal.

In this thesis schematic and layout of a quad-edge-triggered ternary D flip-flop (QETDFF) are introduced. We designed schematic of a ternary serial adder using QETDFF. We simulated average power, clock to Q delay, setup time margin, and hold time margin of QETDFF for all possible cases. Also, we simulated the characteristics of the proposed ternary serial adder. Simulation results show a dramatic improvement over conventional ternary sequential circuits.

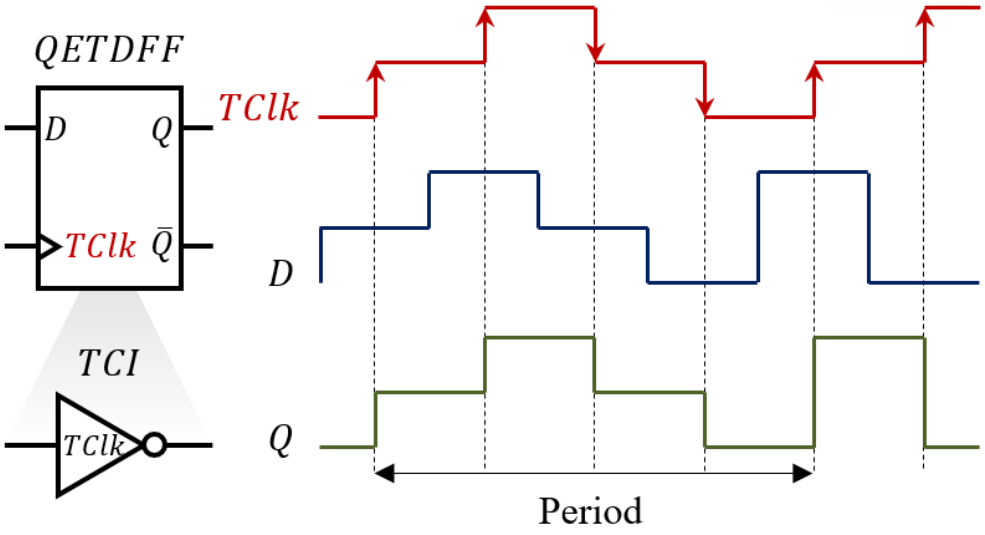


Fig. 2. A ternary sequential circuit which operates at quad-edge of a ternary clock signal. QETDFF can process a ternary clock signal by using the ternary clock inverter (TCI).

The main contributions of our work are as follows:

• We have modeled the characteristics of emerging ternary devices, and proposed an optimal design methodology for static ternary gates using the emerging devices.

• Our proposed methodology can be applied to not only standard ternary logic but also balanced ternary logic.

• We propose a methodology for using ternary values effectively in sequential logic circuits.

• We design a ternary D flip-flop and a ternary serial adder which operates at quad-edges of a ternary clock signal.

• We demonstrate the energy efficiency of our ternary designs over state of the ternary circuits.

The remainder of this thesis is organized as follows. Section II describes the studies related to this thesis. In section III, we model the characteristics of emerging devices for ternary logic synthesis. We propose a methodology for designing optimal ternary logic gates based on modeled ternary devices. In section IV, we propose ternary combinational circuits, which are ternary adder and ternary multiplier. We verify the performance improvement of the ternary circuits designed through the proposed methodology. In section V, we propose a ternary sequential circuit which operates at quad-edges of a ternary clock signal. We verify the performance improvement of the proposed design. We simulated not only QETDFF but also ternary serial adder which use QETDFF. Section VI summarizes and concludes the thesis.

Chapter II

Related Works

2.1 Ternary Device

CNTFET is one of the most remarkable ternary device in recent years. In the structure of CNTFET, semiconducting single-wall carbon nanotubes (SWCNT) is inserted into electronic devices like a structure of MOSFET [18]. The CNTFET operates as a semiconductor or a conductor according to chirality vector. The chirality vector is expressed as pair of an integer (n, m), which means the angle of the arrangement of carbon atoms in the tube. Fig. 3. shows the structure of CNTFET in [21].

An efficient complementary design of standard ternary inverter (STI) using CNTFET is proposed by [19]. This design consists of a parallel connection of two complementary circuits that generate each output value, *VDD*/*GND* and half *VDD*. P-type and N-type CNTFET with a diameter of 1.018 *nm* are diode connected to the output node for generating the half *VDD*. CNTFETs with diameter of 0.783 *nm*, 1.487 *nm* are used to switch each network of the circuits. When the diameter (*DCNT*) of CNTFET is increased, the chirality vector (*n*) is increased, and the threshold voltage (*Vth*) is decreased. The equation shows this relationship.

$$\frac{V_{th1}}{V_{th2}} = \frac{D_{CNT2}}{D_{CNT1}} = \frac{n_2}{n_1}$$

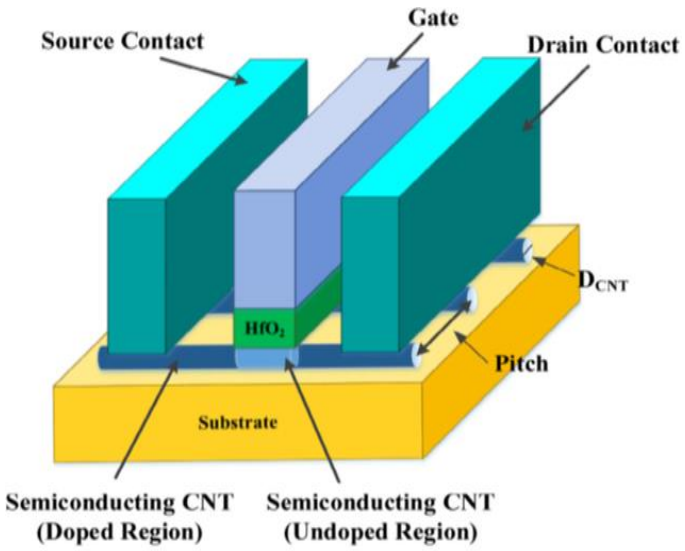
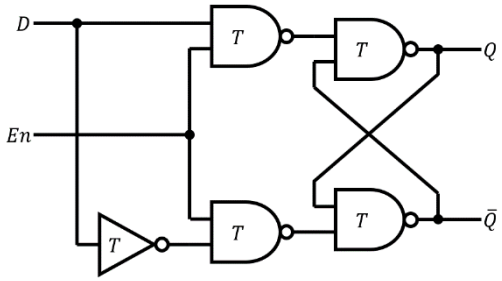


Fig. 3. The structure of MOSFET-like CNTFET [21].

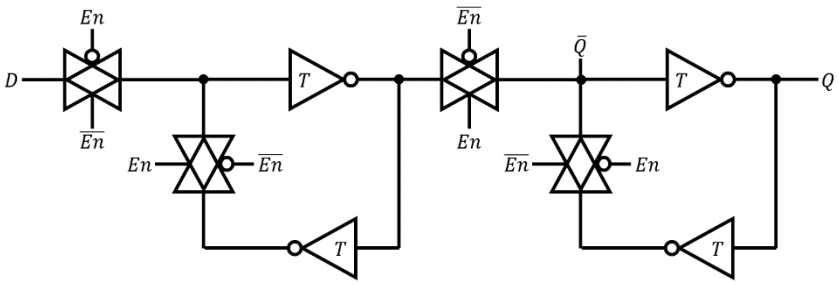
2.2 Ternary Gate

As ternary devices have been studied, various ternary circuit designs have been proposed. Initially, studies were conducted to improve the efficiency of certain ternary circuits such as adder and multiplier. However, design of ternary logic which improve temporal data density has not been studied sufficiently. Several designs of ternary sequential circuit are presented in [20, 21, 22]. In ternary D latch structure of [22], two ternary NMIN gates are cross-coupled to keep input values (S-R latch). Then two additional NMIN gates control operation of the S-R latch according to enable signal. In the case of D latch, STI excludes invalid inputs of S-R latch. However, enable signal can have three states in ternary logic, the operation of D latch is still redundant when enable signal is half *VDD*. In addition, this circuit is designed using MTCMOS and is not compatible with ternary logic using CNTFET.

Another ternary D latch structure using CNTFET is presented by [21]. This structure, two transmission gates control the operation of back-to-back STI gates. A ternary flip-flop design is proposed by serial connection of two ternary latches which have different enable condition. However, these transmission



(a)



(b)

Fig. 4. The gate level schematic of previous (a) Ternary D Latch [22] and (b) Ternary D Flip-Flop [21].

ternary clock signal. Fig. 4. shows gate level schematic of a single-edge-triggered ternary D flip-flop (SETDFF) based on the design of [21, 22].

A design of ternary clock generator was introduced in [23]. This design uses CMOS and generates a ternary clock using the binary clock generated by the quartz multivibrator. The limitation of this design is that the frequency of the generated ternary clock is half of the binary clock. However, it showed a possibility that ternary clock could be generated using an emerging device such as CNTFET in the future.

A multi-valued flip-flop design using MTCMOS that works on a multi-valued clock signal has been proposed by [24]. However, this design is designed using only multiplexers, thus it has limitations in terms of delay and power consumption. Therefore, it is necessary to design a new static ternary sequential circuit using CNTFET for high performance and low power consumption of ternary system.

Chapter III

Methodology of Static Ternary Gate Design

3.1 Characteristic Modeling of Ternary Device

Emerging devices which support a ternary logic include n-type and p-type transistors with different threshold voltages [8]. The operation of the ternary devices can be modeled as an ON/OFF-state switching operation that the flow of current between the source and the drain is controlled according to the gate voltage. The general operation of a CNTFET is the same as CMOS. However, when voltage of the gate is half VDD, the 1.487 nm diameter CNTFET becomes ON-state and the 0.783 nm diameter CNTFET becomes OFF-state. Fig. 5 shows the switching operations of the CNTFET when the gate voltage is half VDD. The different diameters are determined by the chirality vector, with 1.487 nm corresponding to (19, 0) and 0.783 nm corresponding to (10, 0). In addition, a 1.018 nm diameter CNTFET with a chirality vector of (13, 0) has been proposed in [6] for voltage dividing instead of resistance.

The negative ternary inverter (NTI) and positive ternary inverter (PTI) circuits proposed in [6] are connected to gate of the CNTFET devices to implement additional switching operations with a small number of transistors. In addition, by connecting the circuits with proposed switching operations in

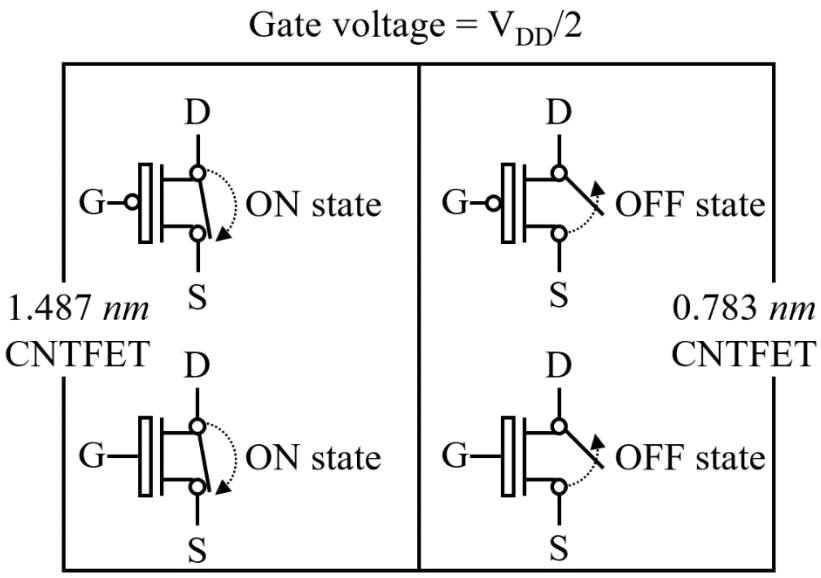


Fig. 5. Switching operation of CNTFETs with different diameters. When the gate voltage is half VDD, the two CNTFETs becomes different ON/OFF states.

series and in parallel, it is possible to implement all kinds of ON/OFF switching operations according to the gate voltage. Fig. 6 shows CNTFETs that can be used for pull-up/down networks. In Fig. 6, I is input value of the gate voltage, IN is input value of the gate voltage through NTI, and IP is input value of the gate voltage through PTI. The input value '0, 1, 2' means the state of voltage (e.g., GND, half VDD, VDD). In this thesis, 1.487 nm, 1.018 nm, and 0.783 nm CNTFET is depicted in blue, green, and red colors, respectively. The switching operator Ai in equations represent the ON/OFF-state of a circuit when a specific input value is received. Conditions with more than one ON-state for certain input values can be expressed as the sum of the switching operators.

$$A_i = \begin{cases} ON-state, & Input = i \\ OFF-state, & otherwise \end{cases}$$

$$A_i + A_j = \begin{cases} ON-state, & Input = i \text{ or } j \\ OFF-state, & otherwise \end{cases}$$

When two or more transistors are connected in series, the pull-up/down networks become ON-state when all transistors are in the ON-state. When two or more transistors are connected in parallel, pull-up/down networks are ON-state even if only one transistor is in the ON-state.

Ternary device switching table				
Pull-up network	(19, 0) I 0.289 *V* 1.487 *nm*	(10, 0) I 0.559 *V* 0.783 *nm*	(19, 0) I_N 0.289 *V* 1.487 *nm*	(19, 0) I_P 0.289 *V* 1.487 *nm*
Pull-down network	(19, 0) I_P 0.289 *V* 1.487 *nm*	(19, 0) I_N 0.289 *V* 1.487 *nm*	(19, 0) I 0.289 *V* 1.487 *nm*	(10, 0) I 0.559 *V* 0.783 *nm*
Switching operation				
Input = 0	ON state	ON state	OFF state	OFF state
Input = 1	ON state	OFF state	ON state	OFF state
Input = 2	OFF state	OFF state	ON state	ON state
Operator	A_0+A_1	A_0	A_1+A_2	A_2

Fig. 6. Ternary device switching table for pull-up/pull-down networks. The modeled switching operation is represented by a switching operator. To implement all switching operations, two or more transistors are connected in series or parallel.

3.2 Single Input Ternary Gate Design

Static gates (complementary gates) have high performance, low power and good noise margins. Generally, static gates are composed of pull-up network connected to VDD with p-type transistor and pull-down network connected to GND with n-type transistor. The ternary logic gates are implemented with two logic paths, which control the output value to be VDD/GND and half VDD separately. Fig. 7 shows the structure of static ternary gate composed of the VDD/GND path and the half VDD path. The VDD/GND path makes the output value to be VDD when the pull-up network becomes ON-state, and the output value to be GND when the pull-down network becomes ON-state. At this time, the pull-up/down networks operate complementarily, such that they do not enter the ON-state at the same time. The pull-up/down networks of the half VDD path simultaneously enter the ON-state, allowing the output value to be half VDD through diode-connected transistors. At this time, VDD/GND path should be OFF-state. To design an optimized static ternary gate, a switching table for the pull-up/down networks should be generated based on a given truth table. The switching table shows the switching conditions of the pull-up/down networks to obtain each output value. The switching table should be generated for VDD/GND path and half VDD path separately. Fig. 8 shows the switching table of a standard ternary inverter (STI), which is a representative example of a static ternary gate. The switching value is indicated as one at the ON-state and zero at the OFF-state. When the pull-up network of the VDD/GND path is ON-state, the pull-up network of the half VDD path can be ON-state or OFF-state. Similarly, when the pull-down network of the VDD/GND path is ON-state, the pull-down network of the half VDD path can be ON-state or OFF state, and it is indicated as ‘X’ (don’t care condition).

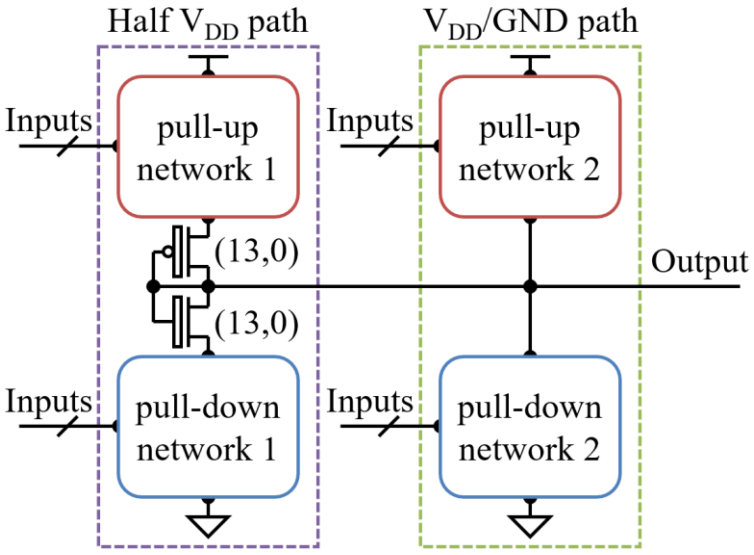


Fig. 7. The structure of the static ternary gate composed of the VDD/GND path and the half VDD path.

The switching table consists of two values which can be converted into a SOP expression. Equations represent SOP expressions which are converted from the switching table. Each switching value is multiplied by switching operators 'A0, A1, A2', and they are added together. Equations represent SOP expression of the half VDD path. Each SOP expression can be calculated as sum of the operators which is multiplied by one. The calculated SOP expression is mapped to the ternary device switching table shown in Fig. 6. The circuit is designed with the pull-up/down networks of each path. The 'X' is considered to use fewer ternary devices. For example, in Fig. 8, STI is synthesized with six transistors when the 'X' of the switching table is ON-state. On the other hand, it is synthesized with eight transistors when it is OFF-state. The sum of operators represents a parallel connection of the transistors, and the product represents a serial connection of the transistors.

$$VDD/GND\ path$$

$$Pull-up\ network: 0*(A_1+A_2)+1*A_0=A_0$$

$$Pull-down\ network: 0*(A_0+A_1)+1*A_2=A_2$$

$$Half\ VDD\ path$$

$$Pull-up\ network: 0*A_2+1*(A_0+A_1)=A_0+A_1$$

$$Pull-down\ network: 0*A_0+1*(A_1+A_2)=A_1+A_2$$

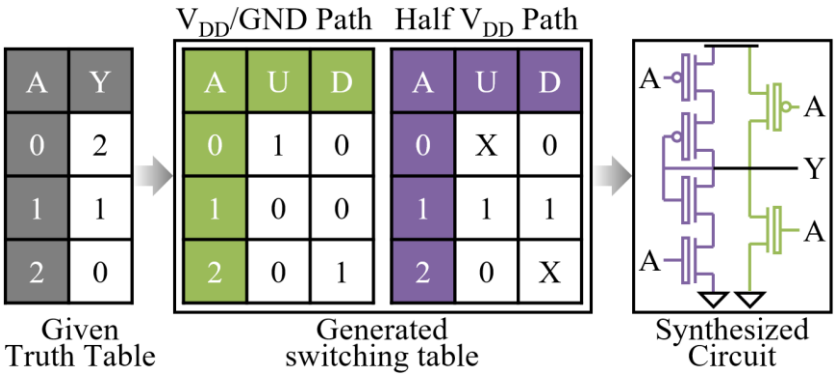


Fig. 8. The pull-up/pull-down switching table of the STI. The synthesized circuit using the proposed methodology is the same as the previously proposed STI circuit.

3.3 Multi-input Ternary Gate Design

The methodology of a single input gate design can be applied to gate designs with more than two inputs. However, we need to minimize a SOP expression, because gates are getting more complicated as the number of input variables increases. Fig. 9 shows the switching table of the pull-up and the pull-down networks for a ternary SUM gate. The switching table can be converted into the SOP expression as shown in equations, and they can be minimized through the modified Quine-McCluskey (Q-M) algorithm [12]. The modified Q-M algorithm weights the minterm with fewer ternary devices to consider the don't care condition 'X'. Fig. 10 summarizes the flow of our static ternary gate design methodology.

$$VDD/GND\ path$$

$$Pull-up\ network: A_0 * B_2 + A_1 * B_1 + A_2 * B_0$$

$$Pull-down\ network: A_0 * B_0 + A_1 * B_2 + A_2 * B_1$$

$$Half\ VDD\ path$$

$$Pull-up\ network: A_0 * (B_1 + B_2) + (A_1 + A_2) * B_0 + A_2 * B_2$$

$$Pull-down\ network\ A_0 * (B_0 + B_1) + (A_0 + A_1) * B_0 + A_2 * B_2$$

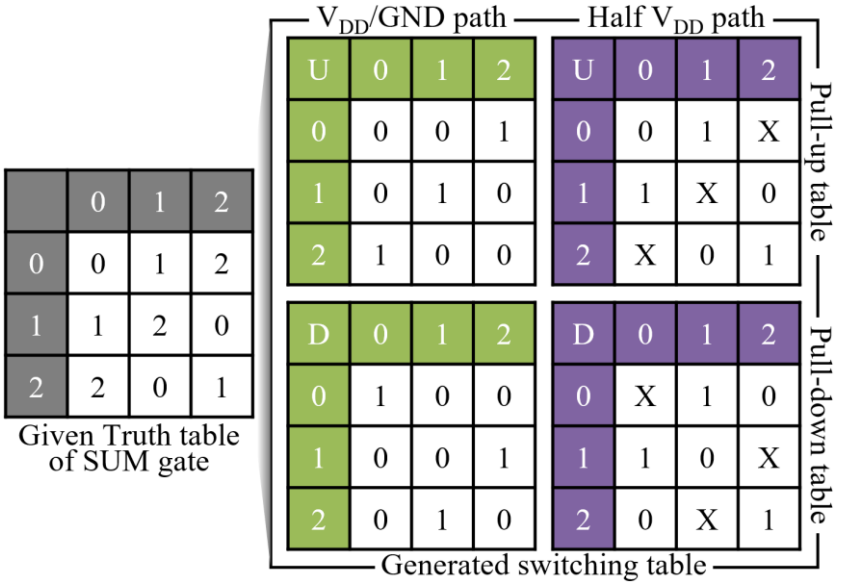


Fig. 9. The pull-up/pull-down switching table of the SUM gate. The proposed methodology applies equally to multi-input gate.

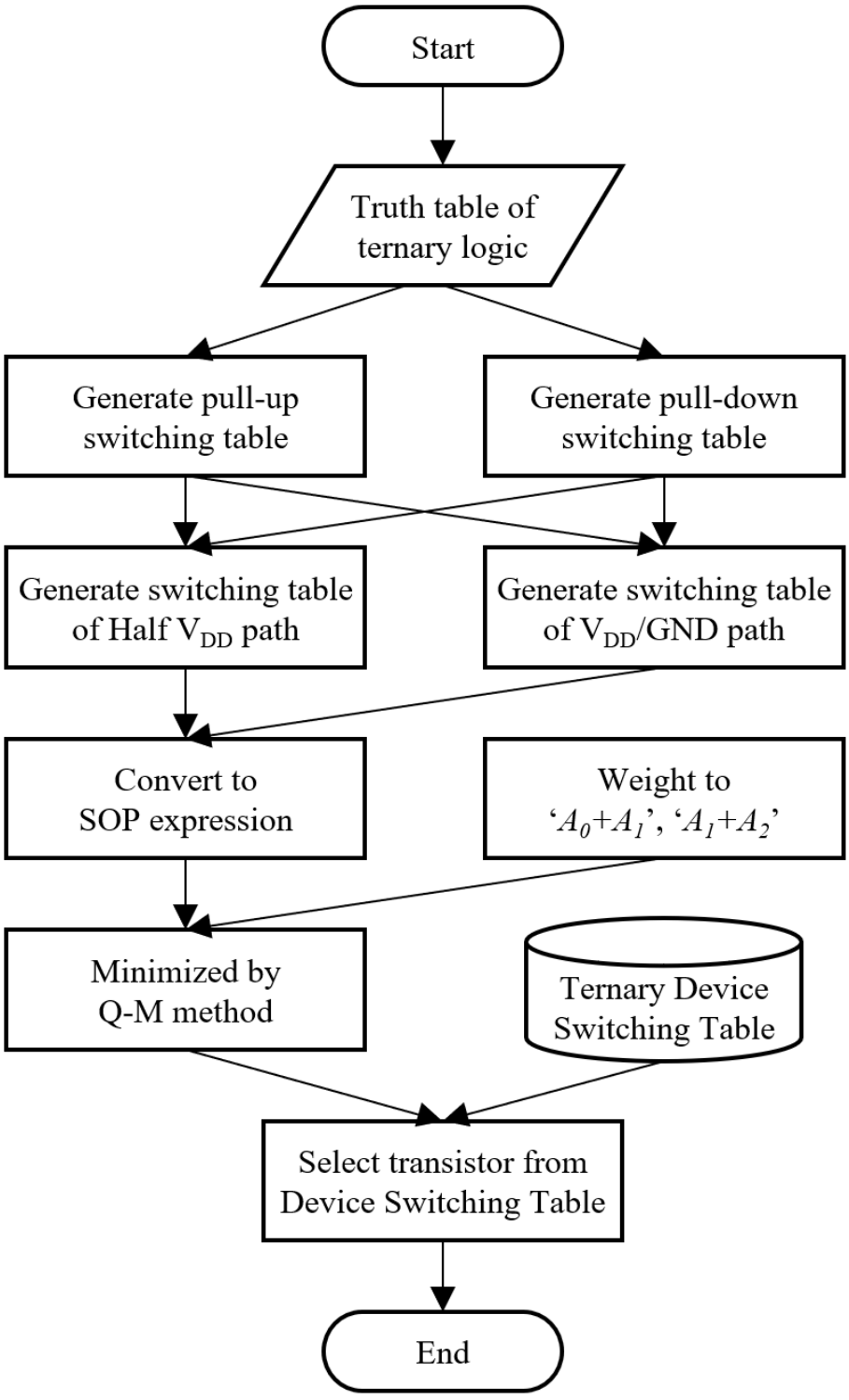


Fig. 10. Flow chart of the static ternary gate design methodology.

Chapter IV

Ternary Combinational Circuit

4.1 Simulation Setup

To analyze our ternary design methodology, we have synthesized several arithmetic logic gates, including the ternary full adder and the ternary multiplier. Fig. 11 shows gate-level schematic of the ternary full adder and the ternary multiplier. This schematic can be used for both standard ternary logic and balanced ternary logic. Table I shows the function of the synthesized gates used in our experiments. Since our methodology is applicable to all emerging devices that support ternary logic, we have synthesized the circuit using the CNTFET and T-CMOS. Our experiments have been carried out by HSPICE simulation [15] using the CNTFET compact model [9]. The VDD is 0.9 V and the input pattern of [11] and 0.01 ns transition time has been used for the simulation. We have measured average power and worst delay for full adders and multipliers. PDP (power-delay product) is calculated with a product of the average power and the worst delay. The simulation results are normalized to our proposed results.

TABLE I
FUNCTION OF TERNARY LOGIC GATE

Logic	Design	Gate	Function
Standard ternary logic	Full adder	SUM	$Sum(A,B) = (A+B)\ mod\ 3$
		NCARRY	$NCarry(A,B) = \begin{cases} 1, & A+B \geq 3 \\ 2, & otherwise \end{cases}$
		NANY	$NAny(A,B) = \begin{cases} 0, & A = B = 2 \\ 2, & A \neq 2\ and\ B \neq 2 \\ 1, & otherwise \end{cases}$
	Multiplier	PRODUCT	$Prod(A,B) = (A \cdot B)\ mod\ 3$
		CARRY	$Prod\ Carry(A,B) = \begin{cases} 1, & A = B = 2 \\ 0, & otherwise \end{cases}$
Balanced ternary logic	Full adder	SUM	$Sum(A,B) = \begin{cases} -1, & A+B > 1 \\ 1, & A+B < -1 \\ A+B, & otherwise \end{cases}$
		NCARRY	$NCarry(A,B) = \begin{cases} -1, & A = B = 1 \\ 1, & A = B = -1 \\ 0, & otherwise \end{cases}$
		NANY	$NAny(A,B) = \begin{cases} -1, & A+B > 0 \\ 1, & A+B < 0 \\ 0, & otherwise \end{cases}$
	Multiplier	PRODUCT	$Prod(A,B) = A \cdot B$

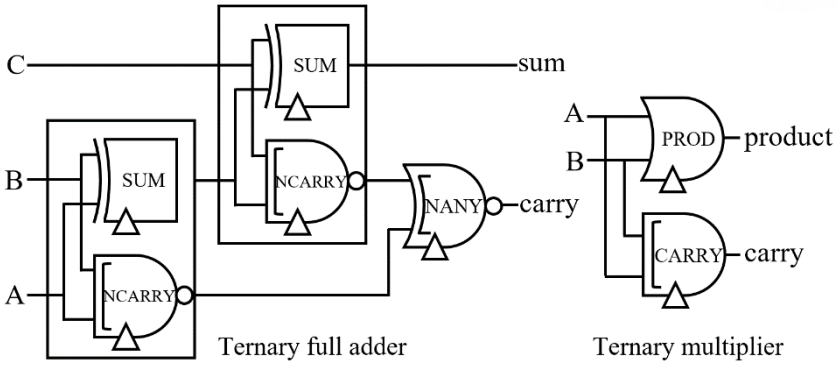


Fig. 11. The gate-level schematic of the ternary full adder and ternary multiplier.

4.2 Ternary Full Adder Design & Simulation Result

Balanced ternary logic is an efficient notation to present a signed ternary arithmetic [13], [14]. To implement signed ternary arithmetic logic with standard ternary logic, we need to use 3's complement. Then, a sign trit can take logic value zero and two, and it reduces the number of representations to one third. On the other hand, one trit of balanced ternary logic consists of 1, 0, and -1, so signed ternary

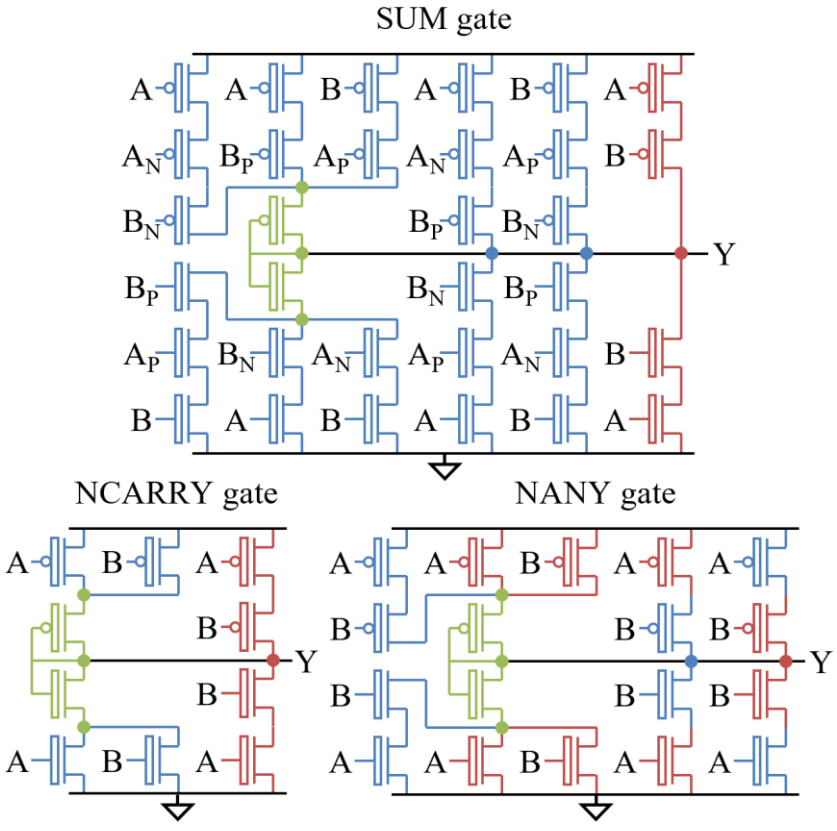


Fig. 12. The transistor-level schematic of the gates for balanced ternary full adder using CNTFET.

arithmetic logic can be implemented without loss of a sign trit. Fig. 12 shows the transistor-level schematic of the balanced ternary full adder using CNTFET.

Standard ternary full adder consists of two half adders and NANY gate, and one-half adder consists of one SUM gate and one NCARRY gate. Fig. 13 shows the transistor-level schematic of the standard ternary full adder using CNTFET. Table II compares the normalized worst delay, average power, and PDP results of ternary full adder. Our proposed design shows 49 % PDP reduction compare to the design of [7], which is based on a transmission gate. Moreover, our proposed design shows 79 % PDP reduction compare to the design of [11]. Fig. 14 shows reduction rate of the normalized PDP of proposed designs compare to the previous works for each load capacitors, 2 fF and 3 fF. It can be seen that the static gates used in the proposed design are more efficient than the gates proposed in the previous works.

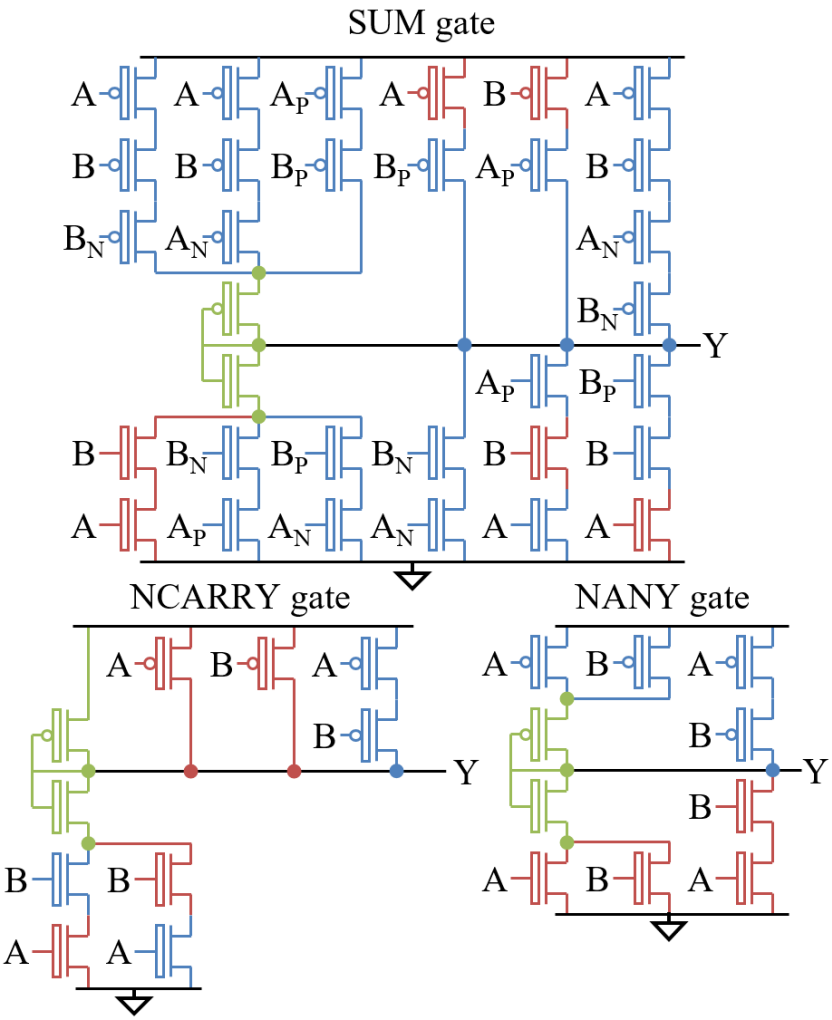


Fig. 13. The transistor-level schematic of the gates for standard ternary full adder using CNTFET.

TABLE II
COMPARISON OF TERNARY FULL ADDER DESIGN

Design	Load Cap. (*fF*)	Normalized Delay	Normalized Power	Normalized PDP
[10]	2	1.58	16.98	27.02
[10]	3	1.30	17.05	22.31
[11]	2	0.93	5.90	5.49
[11]	3	0.66	6.15	4.06
[7]	2	0.71	2.76	1.96
[7]	3	0.73	2.70	1.98
Proposed	2	1.00	1.00	1.00
Proposed	3	1.00	1.00	1.00

TABLE III
COMPARISON OF TERNARY MULTIPLIER DESIGN

Design	Load Cap. (*fF*)	Normalized Delay	Normalized Power	Normalized PDP
[7]	2	1.03	2.63	2.71
[7]	3	1.02	2.47	2.53
Proposed	2	1.00	1.00	1.00
Proposed	3	1.00	1.00	1.00

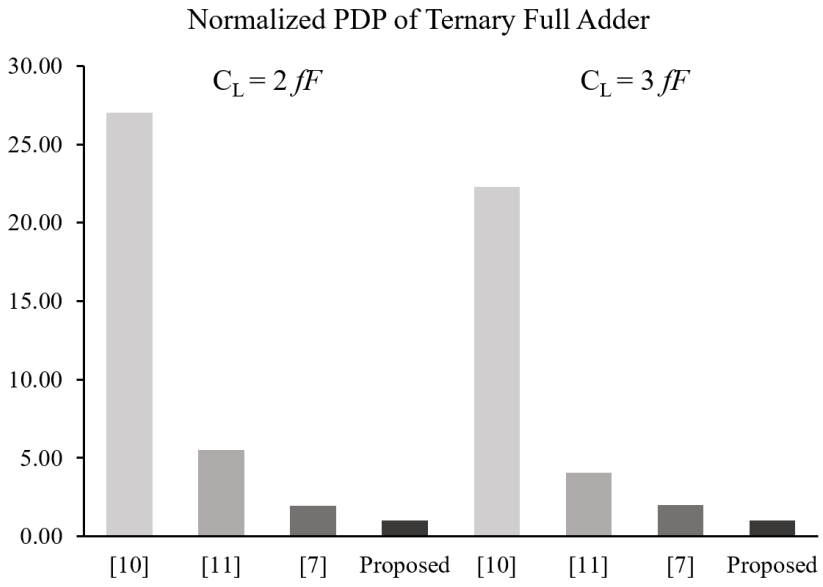


Fig. 14. Comparison of normalized PDP to each design for load capacitors 2 fF and 3 fF.

4.3 Ternary Multiplier Design & Simulation Result

A single-trit ternary multiplier based on standard ternary logic consists of a product gate and a carry gate. The proposed ternary multipliers have been significantly improved over previous designs. Table III shows comparison of the normalized worst delay, average power, and PDP results between ternary multipliers. From the results, we can see that our proposed design has significantly reduced the data path delay and required number of devices compared to design in [7]. Our proposed design shows 62 % PDP reduction compared to the previous work [7]. We have also implemented a single trit multiplier based on the balanced ternary logic. Compared to the standard ternary multiplier, the benefit of balanced design is that it has only one output. The reason is that one trit of balanced ternary logic is composed of 1, 0, -1 and the multiplication result does not make a carry trit. Fig. 15 shows the number of transistors with different digit size of the signed multiplier. We have implemented a multidigit multiplier based on an array multiplier structure using CMOS and T-CMOS. From the experimental results, we can see that ternary multiplier shows smaller number of elements over the binary multiplier, especially on the large digit size.

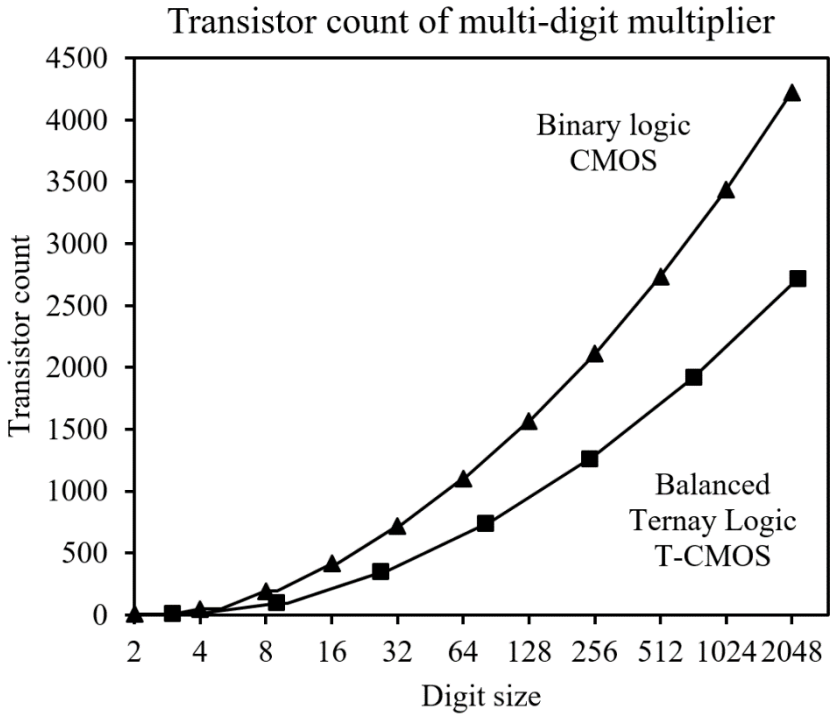


Fig. 15. The number of transistors that increase as the digit size of the signed multiplier.

Chapter V

Ternary Sequential Circuit

5.1 Quad-Edge-Triggered Ternary Sequential Circuit

Quad-edge-triggered ternary D flip-flop design consists of four logic gates inverter (INV), standard ternary inverter (STI), transmission gate (TG), and ternary clock inverter (TCI). The transistor level schematic and symbol of each gate are shown in the Fig. 16. The structure of STI is proposed in [6]. A CNTFET with a diameter of 1.487 nm is used for the fast operation of inverter and transmission gate. Ternary clock inverter is designed as a static gate to satisfy the truth table of Table IV.

The enable signal that controls the operation of transmission gate consists of *VDD* and *GND*. Inverted enable signal is generated from the inverter. When the enable signal is half *VDD*, the *VGS* of transmission gate is low, and transmission speed becomes slow. Therefore, we did not input ternary

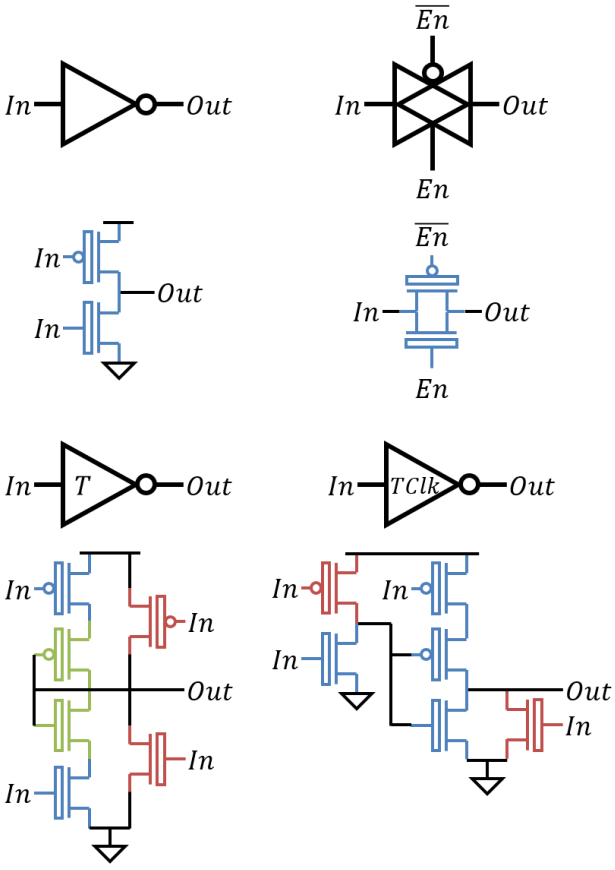


Fig. 16. The transistor level schematic of logic gates which are used QETDFF.

TABLE IV
TRUTH TABLE OF TERNARY GATES

INV		**STI**		**TCI**		**TG**	
In	*Out*	*In*	*Out*	*In*	*Out*	*En*	*Out*
0	2	0	2	0	0	0	Z
1	N/A	1	1	1	2	1	N/A
2	0	2	0	2	0	2	In

clock signal directly into the transmission gate. Ternary clock signal is entered to ternary clock inverter. TCI converts a ternary clock signal to a binary enable signal. The truth table of ternary clock inverter is shown in Table IV. The gate level schematic of QETDFF is shown in Fig. 17. Two ternary D latches whose output value is controlled by a transmission gate are connected in parallel to the input node and the inverted output nodes. The operation of ternary D latch consists of two phases: the first phase is writing a value into the circuit, and the second phase is transmitting the written value to the output STI.

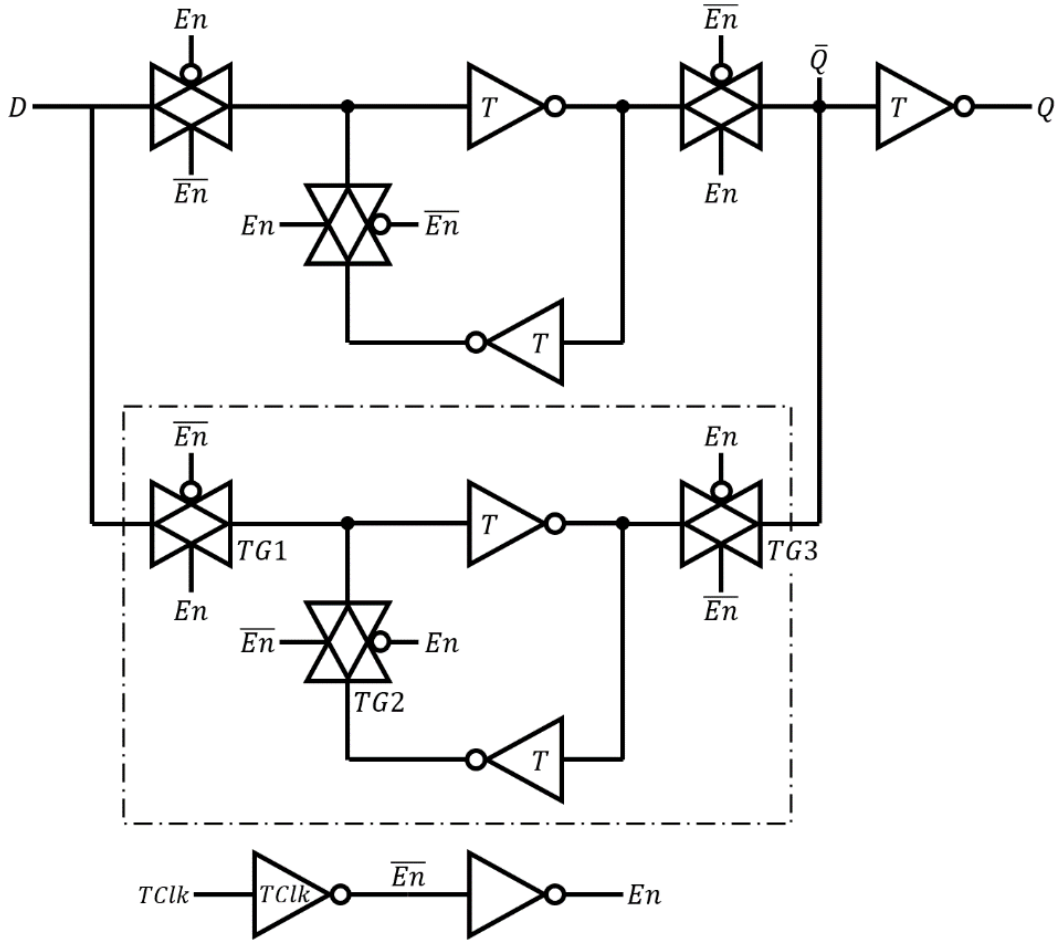


Fig. 17. The gate level schematic of QETDFF.

TABLE V
TRUTH TABLE OF QETDFF

$TClk$	En	$\overline{En}$	D	$Q(t+1)$	$\overline{Q(t+1)}$
1→0 or 1→2 (From Half V_{DD} Edge)	0→2	2→0	0	0	2
			1	1	1
			2	2	0
0→1 or 2→1 (To Half V_{DD} Edge)	2→0	0→2	0	0	2
			1	1	1
			2	2	0
Otherwise			X	$Q(t)$	$\overline{Q(t)}$

In the first phase, the enable signal is *VDD*, and TG1 transmits a value from the input node to back-to-back STI. Because inverted enable signal is *GND*, TG2 disconnects the loop of back-to-back STI, and the transmitted value can be written. At this time TG3 disconnects the path to the inverted output node, and the written value cannot be transmitted to the output STI. In the second phase, enable signal is *GND*, TG1 blocks an input value. Because inverted enable signal is *VDD*, TG2 connects the loop of back-to-back STI. At this time, the written value which is transmitted by TG1 in first phase is strongly held by the back-to-back STI. Then TG3 transmits the written value from back-to-back STI to the inverted output node. The output STI stably transfers the transmitted value to the next circuit.

Two ternary D latches whose output value are controlled by a transmission gate always receive different enable signals. Thus, they are always in different phases. Inverted enable signal is generated from a ternary clock signal using ternary clock inverter. Inverted enable signal is *VDD* when the ternary clock signal is half *VDD*, otherwise, it is *GND*. Enable signal is generated from the inverted enable signal using an inverter. Thus, enable signal is *GND* when the ternary clock signal is half *VDD*, otherwise, it is *VDD*. Therefore, QETDFF can respond to all edges of the ternary clock signal because the latch that respond to 'From Half *VDD* Edge' and the latch that respond to 'To Half *VDD* Edge' operate alternately. The operation of QETDFF is shown Table V. The Fig. 19. shows the transition response of QETDFF.

The layout of QETDFF, shown in Fig. 18., followed the CNTFET layout technique from [25]. In this layout, the only metal 1 is visualized and the λ-based scale is used for normalizing the size. Especially, the distance between the pull-up network and the pull-down network in this CNTFET layout is just 3λ which is quite short distance compared to 10λ in normal CMOS layout. The area of QETDFF is 106λ × 67λ (7102λ2). The area of TCI and Inverter are 51λ × 20λ (1020λ2).

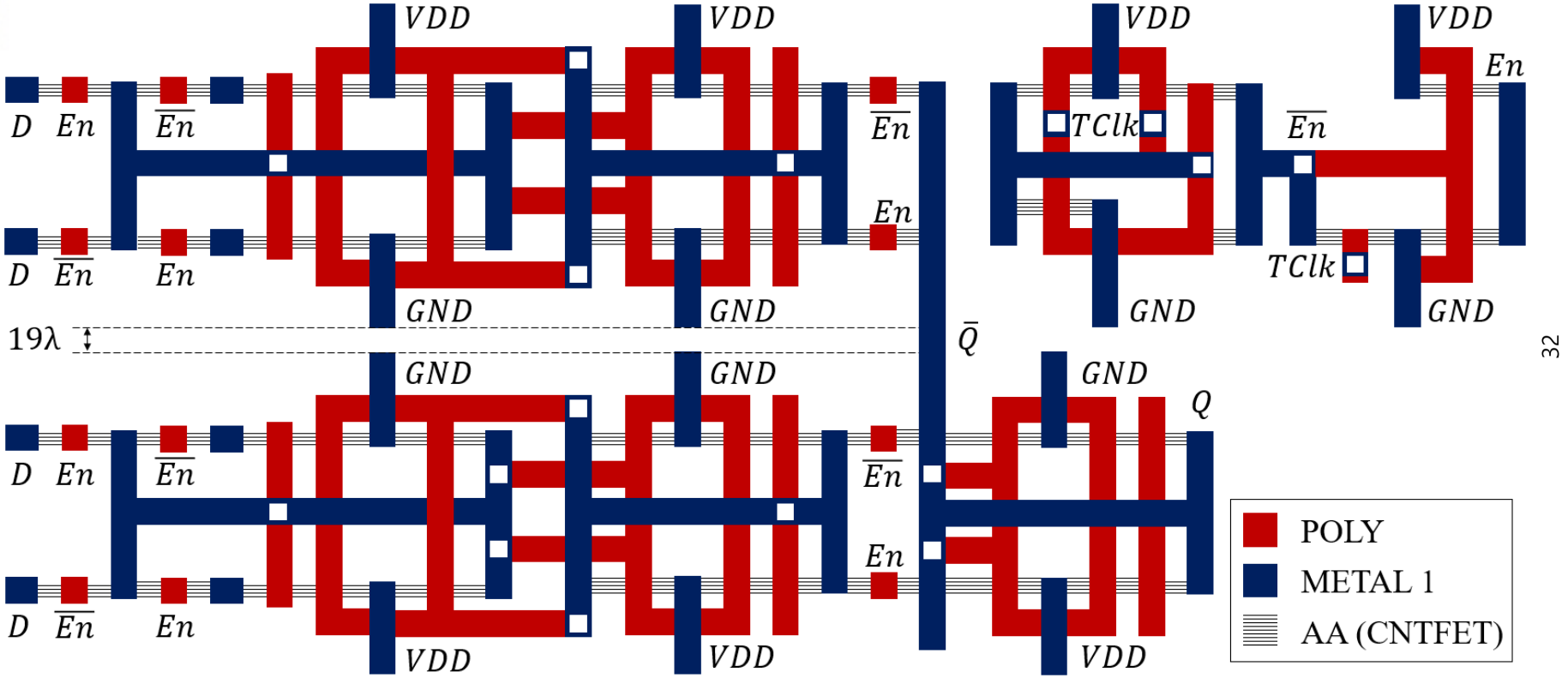


Fig. 18. The layout of QETDFF.

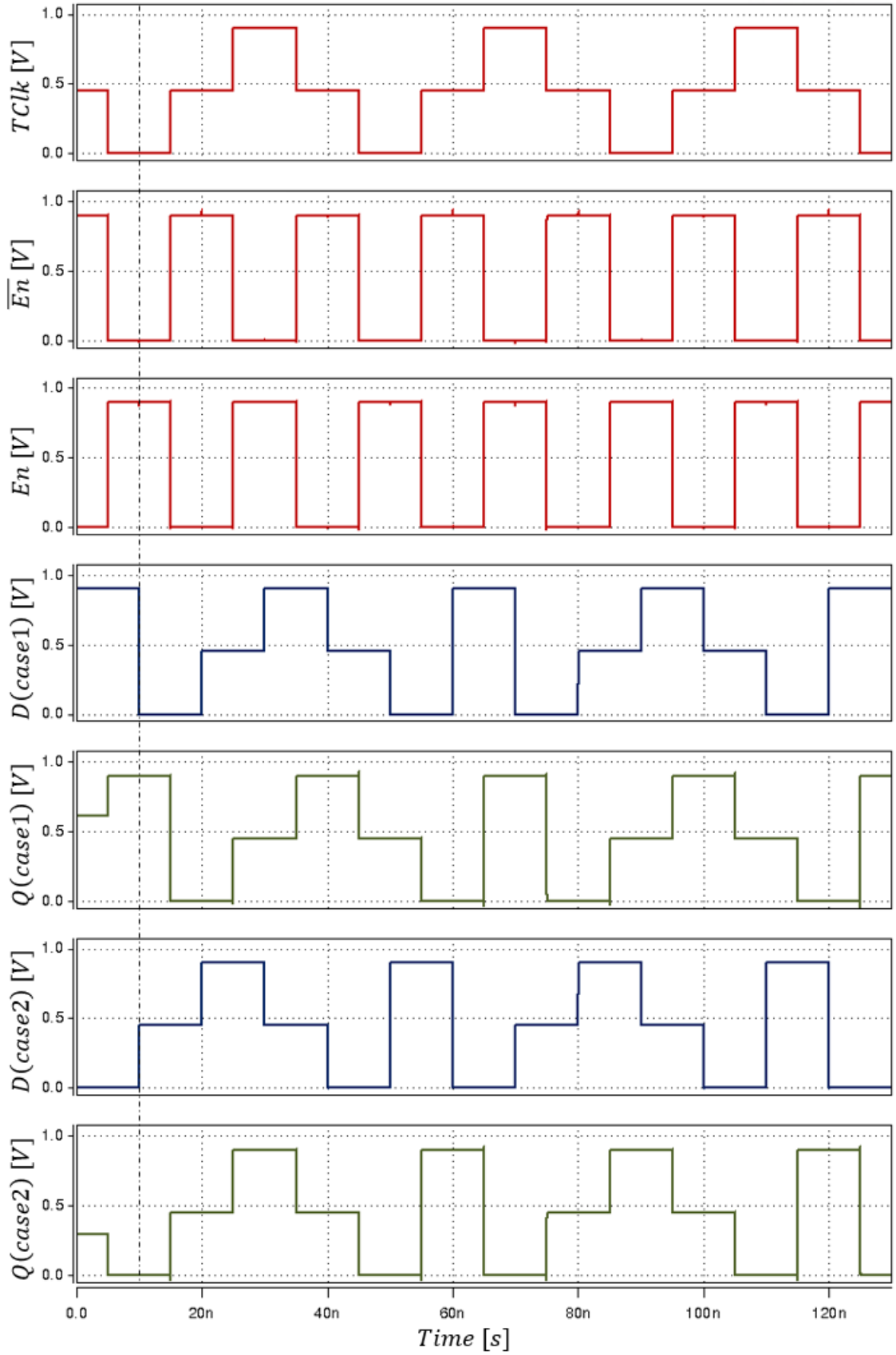


Fig. 19. The transient response of QETDFF.

5.2 Simulation Setup

To analyze the characteristic of proposed design, we carried out HSPICE simulation using CNTFET compact model [9]. The *VDD* is 0.9 *V* and transition time is 0.01 *ns*. To analyze the behaviors of sequential circuit in all cases, we used the input pattern shown in Fig. 19. Case 1 and case 2 contain the patterns of all output values that can be changed on each edge. In order to prevent duplication of the patterns, two cases were separately simulated. We measured the average power consumption and the clock to Q delay. We calculated the power-delay-product (PDP) which is product of the worst delay and the average power consumption of circuits. Total energy consumption which is the product of a total simulation time and the average power consumption was calculated. The average power consumption and the energy consumption were measured from 10 *ns* to 130 *ns* to exclude initial values in the simulation of QETDFF. Thus, total simulation time is 120 *ns*. Important CNTFET parameters used in the simulation are shown in Table VI. Although enhanced performance was obtained when parameters of [21] was applied, we simulated using the default parameters.

TABLE VI
IMPORTANT PARAMETERS OF THE CNTFET MODEL

Parameter	Value
Physical channel length	32 *nm*
The mean free path in the intrinsic CNT	200 *nm*
The length of doped CNT drain-side region	16 *nm*
The length of doped CNT source-side region	16 *nm*
The mean free path in P^+/n^+doped CNT	15 *nm*
The distance between the centers of two adjacent CNTs within the same gate	20 *nm*
Sub-lithographic pitch	6.4 *nm*
The thickness of high-k top gate dielectric	4 *nm*
The dielectric constant of high-k top gate dielectric material(HfO_2)	16
The dielectric constant of substrate(SiO_2)	4
The coupling capacitance between channel region and the substrate(SiO_2)	40 *aF/um*
The Fermi level of the doped S/D CNT	0.66 *eV*
The work function of S/D metal contacts	4.5 *eV*
CNT work function	4.5 *eV*

5.3 Simulation Results of QETDFF

The transient response of QETDFF is shown in Fig. 19. The waveforms show the correct and fast operations of the QETDFF. We moved the transient timing of the input signal to find a setup time margin and a hold time margin. The setup time margin of QETDFF is 7 *ps* and the hold time margin is 11 *ps*. Table VII shows the clock to Q delay for each clock edge according to all possible output values of QETDFF. The unit of the clock to Q delay is *ps*. The worst delay condition is that the ternary clock signal changes from zero to one and the output value changes from zero to one. It is because CNTFET with a diameter of 1.018 *nm* makes delay in generating half *VDD*.

Table VIII shows the worst delay, the power consumption, and the PDP results of QETDFF with another ternary flip-flop. In comparison with the design of [20], the worst delay improved 78.91 % and the power consumption improved 16.1 %, and the PDP improved 82.31 %. In comparison with transmission gate based flip-flop design of [21] which is shown in the Fig. 4., the worst delay improved 91.37 % and the power consumption improved 33.4 %, and the PDP improved 94.25 %. It is because QETDFF is designed as a static logic gate. Also, QETDFF can be designed with a smaller area, since capacitors are not used. As mentioned earlier, when a ternary clock signal can be generated using a sinusoidal signal, the total power consumption of QETDFF can be reduced to 1/4 compared with a single-edge-triggered ternary flip-flop using a binary clock signal. On the other hand, a ternary digital system with QETDFF can reduce the clock frequency to improve power consumption and delay of sequential circuits.

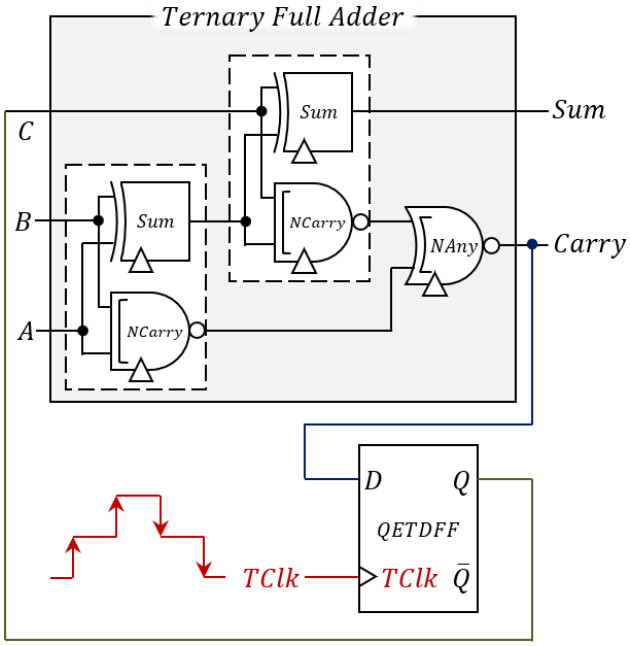


Fig. 20. The gate level schematic of proposed ternary serial adder.

5.4 Simulation Results of Ternary Serial Adder

Sequential circuits are used with combinational circuits to construct synchronous digital circuits. Arithmetic logic unit (ALU) is a typical example, in which adder or multiplier circuits are operate in synchronization with a clock signal. We design a serial adder as shown Fig. 20. to analyze the behaviors and the characteristics of QETDFF. The ternary full adder design used in the simulation is proposed in [21]. As shown in the Fig. 21., three types of gates and two types of inverters are used to design the ternary full adder. Since all gates are designed as static gates using CNTFET, they are optimized for performance and power consumption. The frequency of the ternary clock signal used in QETDFF is 25 *MHz* and the clock signal are 7 *ps* faster than the input signals to ensure a setup time margin.

Fig. 22. shows the transient response of the proposed ternary serial adder. The waveforms show that the operation of the proposed ternary serial adder is fast and accurate, with few glitches generated at setup time margin. Table IX shows worst delay, power consumption, and PDP results of proposed design with other ternary serial adder designs. In comparison with the design of [21], the worst delay improved

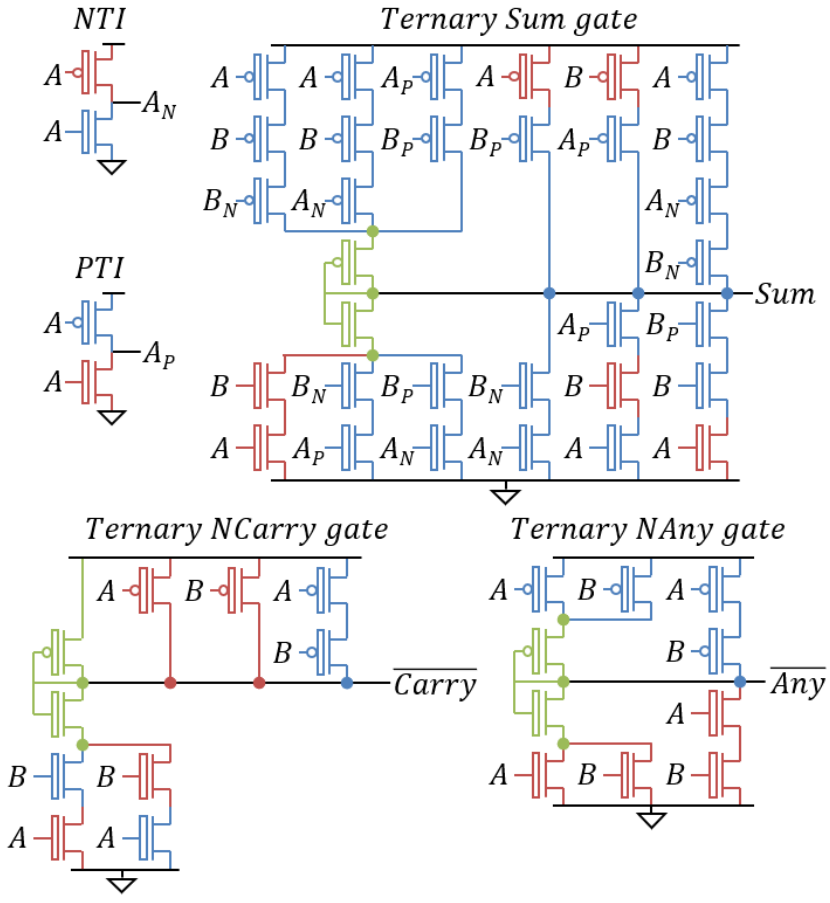


Fig. 21. The transistor level schematic of logic gates which are used in ternary full adder.

67.03 % and the power consumption improved 94.6 %, and the PDP improved 98.23 %. It is because many capacitors are used in the design of [21] and the circuit is not designed with a static gate. On the other hand, the proposed design was able to reduce the PDP to 1/56 because both the ternary serial adder and ternary sequential circuit were designed with static gates. Also, the performance of QETDFF contributes to improvement.

TABLE VII
CLOCK TO Q DELAY OF TERNARY FLIP-FLOP DESIGN

Q \ $TClk$	$0 \rightarrow 1$	$1 \rightarrow 2$	$2 \rightarrow 1$	$1 \rightarrow 0$
$0 \rightarrow 1$	24.6	18.70	21.00	13.0
$1 \rightarrow 2$	16.0	13.8	14.7	16.0
$2 \rightarrow 1$	24.0	17.0	21.6	10.0
$1 \rightarrow 0$	18.0	13.0	17.0	8.0
$0 \rightarrow 2$	23.0	16.0	19.0	11.0
$2 \rightarrow 0$	22.7	17.0	19.0	11.0

TABLE VIII
COMPARISON OF TERNARY FLIP-FLOP DESIGN

Design	Worst Delay [ps]	Average Power [uW]	PDP [mJ]
Proposed	24.60	1.00	24.60
[20]	116.66	1.18	137.66
[21]	489.30	2.51	1228.14
[22]	284.92	1.49	424.53

TABLE IX
COMPARISON OF TERNARY SERIAL ADDER DESIGN

Design	Worst Delay [ps]	Average Power [uW]	PDP [mJ]
Proposed	66.00	1.53	101.18
[21]	200.17	28.49	5702.84
[11]	292.43	22.44	6562.13
[16]	307.01	22.64	7564.73

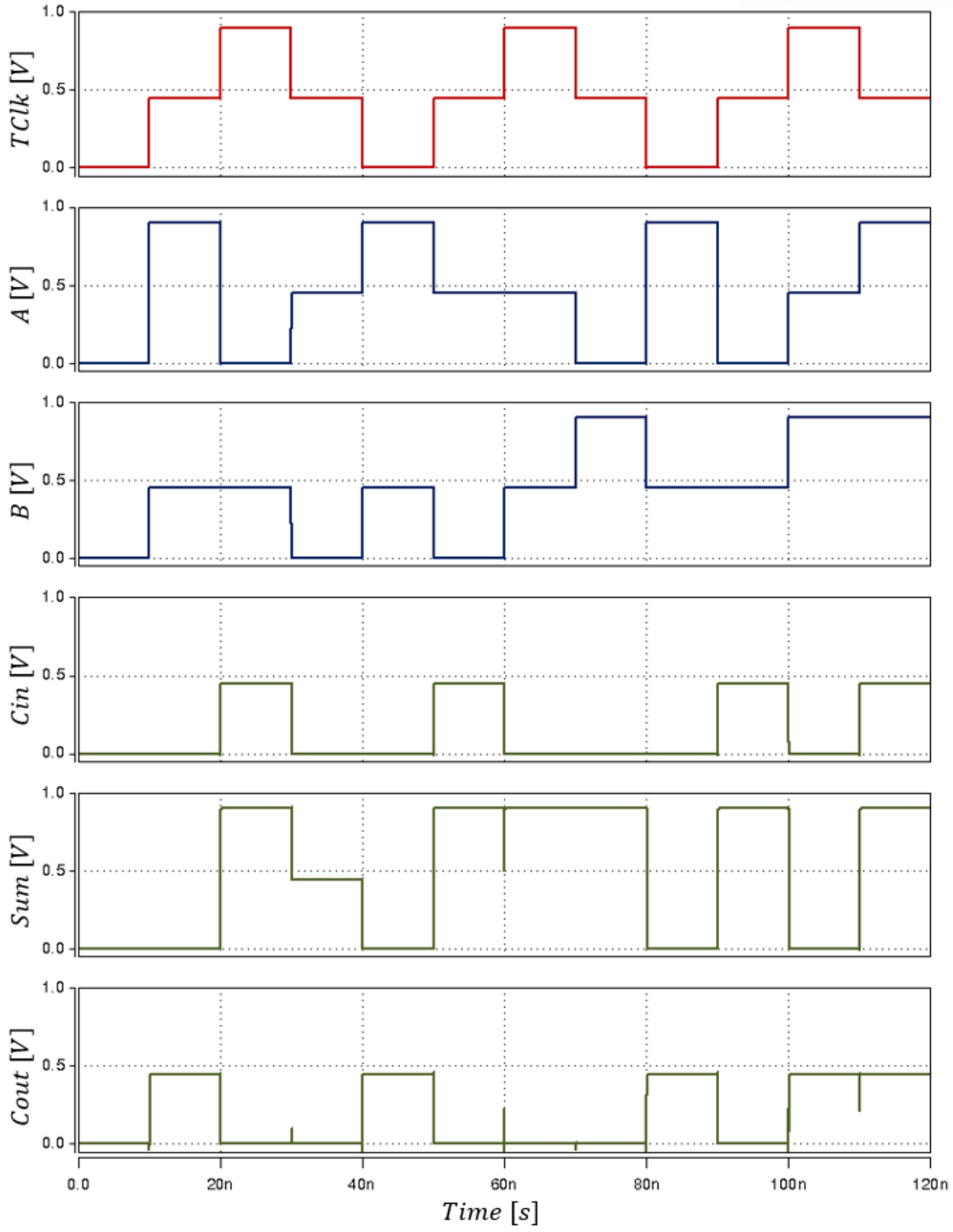


Fig. 22. The transient response of proposed ternary serial adder.

Chapter IV

Conclusion

In this thesis, we propose an optimized gate design methodology for the synthesis of ternary logic circuits. Our proposed methodology can be applied to all emerging devices that support ternary logic (e.g., CNTFET, QDGFET and T-CMOS). Using our ternary gate design technique, it is possible to synthesize ternary logic circuits with various gates. In addition, gates for balanced ternary logic circuits, which have not been studied much in the previous researches, can be implemented optimally. Our design methodology can synthesize ternary gates with a minimum number of transistors. From our experimental results, our ternary designs show significant power delay product reductions compared to the existing methodologies. We have also compared the number of transistors in our ternary circuits with CMOS-based binary logic circuits, and observed that ternary logic circuits have area benefits with increasing digit sizes. Also, we propose a methodology for using ternary clock signal. An efficient sequential circuit is indispensable to implement a system level circuit of ternary logic. It was shown that QETDFF is an effective ternary sequential circuit. The QETDFF increases not only spatial data density but also temporal data density of ternary system. It is hoped that various ternary circuits will be studied with sequential circuits.

REFERENCES

[1] Y. Taur, "CMOS Design near the Limit of Scaling," IBM Journal of Research and Development, 46(2.3) (2002) pp.213-222.

[2] A. Heung and H. T. Mouftah, "Depletion/Enhancement CMOS for a Low Power Family of Three-Valued Logic Circuits," IEEE JSSC, 20(2) (1985) pp.609-616.

[3] S. Lin, Y.-B. Kim, and F. Lombardi, "Design of a Ternary Memory Cell using CNTFETs," IEEE Trans. Nanotechnology, 11(5) (2012) pp.1019- 1025.

[4] S.Kamakar, J.A.Chandy, and F.C.Jain, "Design of Ternary Logic Combinational Circuits based on Quntum Dot Gate FETs," IEEE Trans. VLSI Systems, 21(5) (2013) pp.793-806.

[5] S.Shin, E.Jang, J.W.Jeong, B.G.Park, and K.R.Kim, "Compact Design of Low Power Standard Ternary Inverter based on OFF-State Current Mechanism using Nano-CMOS Technology," IEEE Trans. Electron Devices, 62(8) (2015) pp.2396- 2403.

[6] S. Lin, Y. B. Kim, and F. Lombardi, "CNTFET-Based Design of Ternary Logic Gates and Arithmetic Circuits," IEEE Trans. Nanotechnology, 10(2) (2011) pp.217225.

[7] B. Srinivasu, K. Sridharan, "A Synthesis Methodology for Ternary Logic Circuits in Emerging Device Technologies" IEEE TCAS-1, PP(99) (2017) pp.1-14.

[8] A. Raychowdhury and K. Roy, "Carbon-nanotube-based voltage-mode multiple-valued logic design," IEEE Trans. Nanotechnology, 4(2) (2005) pp.168-179.

[9] J. Deng and H. S. P. Wong, "A compact SPICE model for carbon-nanotube field-effect transistors including nonidealities and its application Part I: Model of the intrinsic channel region," IEEE Trans. Electron Devices, 54(12) (2007) pp.31863194.

[10] M. H. Moaiyeri, R. F. Mirzaee, K. Navi, and O. Hashemipour, "Efficient CNTFET-based ternary full adder cells for nanoelectronics," Nano-Micro Lett., 3(1) (2011) pp.4350.

[11] P. Keshavarzian and R. Sarikhani, "A novel CNTFET-based ternary full adder," Circuits Syst. Signal Process., 33(3) (2014) pp.665679.

[12] E. J. McCluskey, “Minimization of Boolean functions” The Bell System Technical Journal, 289(35) (1956) pp.1417-1444.

[13] H. Gundersen, Y. Berg, “A Balanced Ternary Multiplication Circuit Using Recharged Semi-Floating Gate Devices,” NORCHIP, (2006), pp.205- 208.

[14] D. W. Jones, (2012, Apr 1). The Ternary Manifesto. Retrieved from http://homepage.divms.uiowa.edu/jones/ternary/

[15] Hspice Reference Manual http://www.synopsys.com/

[16] P. C. Balla and A. Antoniou, “Low power dissipation MOS ternary logic family,” *IEEE J. Solid-State Circuits*, 19(5) (1984) pp.739–749.

[17] Y. Yasuda, Y. Tokuda, S. Taima, K. Pak, T. Nakamura, and A. Yoshida,“Realization of quaternary logic circuits by n-channel MOS devices,” *IEEE J. Solid-State Circuits*, 21(1) (1986) pp.162–168.

[18] J. Appenzeller, “Carbon nanotubes for high-performance electronics-Progress and prospect,” Proc. IEEE, 2008, pp. 201–211.

[19] Sheng Lin, Yong-Bin Kim, and Fabrizio Lombardi, “A Novel CNTFET-Based Ternary Logic Gate Design,” Proc. Circuits and Systems, 2009, pp.435–438

[20] Reza Faghih Mirzaee and Niloofar Farahani, “Design of a Ternary Edge-Triggered D Flip-Flap-Flop for Multiple-Valued Sequential Logic,” Journal of Low Power Electronics, 13(1) (2017) pp.36-46

[21] M. H. Moaiyeri, M. Nasiri, and N. Khastoo, “An efficient ternary serial adder based on carbon nanotube FETs,” Engineering Science and Technology, an Int. J., 19(1) (2016) pp. 271–278.

[22] A. P. Dhande and V. T. Ingole, “Design of 3-valued R-S & D flip-flops based on simple ternary gates,” Int. J. Software Engineering and Knowledge Engineering, 15(2) (2005) pp. 411–417.

[23] Yan-Feng Lang, Ji-Zhong Shen, Liang Geng and Mao-Qun Yao, “Design of ternary clock generator,” Electronics Letters, 50(15) (2014) pp. 1052–1054

[24] Yan-Feng Lang & Ji-Zhong Shen, “A general structure of all edges triggered flip flop based on multivalued clock,” International Journal of Electronics, 100(12) (2013) pp.1637–1645

[25] D. Atienza, S. K. Bobba, M. Poli, G. De Micheli, and L. Benini, “Systemlevel design for nano-electronics,” Proc. 14th IEEE Int. Conf. Electron., Circuits Syst., 2007, pp. 747–751.

[26] S.A. Ebrahimi, P. Keshavarzian, S. Sorouri, M. Shahsavari, “Low power CNTFET based ternary full adder cell for nanoelectronics,” Int. J. Soft Comput. Eng., 2(2) (2012) pp.291–295.